Amendments to the Claims:

Claims 1 to 23 (Canceled)

24. (New) A method for implementing an analog-to-digital converter (ADC) for an analog front end circuit of an image processing system, comprising:

de-activating stages of an analog-to-digital converter (ADC) for an analog front end circuit of an image processing system during a reduced resolution mode.

25. (New) The method according to Claim 24, wherein de-activating stages of an analog-to-digital converter (ADC), further comprises:

de-activating lower stages which provide lower significant bits of a digital value.

26. (New) The method according to Claim 25, wherein de-activating lower stages further comprises:

setting the lower significant bits to low values wherein the lower stages in effect contain no information.

27. (New) The method according to Claim 24, wherein the reduced resolution mode is a preview operational mode and de-activating stages of an analog-to-digital converter (ADC), further comprises:

de-activating stages of the ADC during the preview operational mode.

28. (New) The method according to Claim 24, further comprising:

outputting two bits from each of the stages;

outputting a bit significance of a least significant bit and a least significant bit plus one for a most significant bit stage;

outputting another bit significance of twice an output value of a subsequent stage for each of the other stages; and

outputting bits for the ADC by adding together the outputs of all of the stages.

29. (New) An analog-to-digital converter (ADC) for an analog front end circuit of an image processing system, comprising:

analog-to-digital converter (ADC) stages for the ADC wherein at least some of the ADC stages are de-activated during a reduced resolution mode.

30. (New) The ADC according to Claim 29, wherein lower ADC stages which provide lower significant bits of a digital value are de-activated.

31. (New) The ADC according to Claim 30, wherein the lower significant bits are set to low values and the lower ADC stages in effect contain no information.

32. (New) The ADC according to Claim 29, wherein the reduced resolution mode is a preview operational mode.

33. (New) The ADC according to Claim 29, wherein:

each of the stages outputs two bits;

a most significant bit stage outputs a bit significance that is a least significant bit and a least significant bit plus one;

each of the other stages outputs another bit significance that is twice an output value of a subsequent stage; and

the ADC provides output bits by adding together the outputs of all of the stages.

34. (New) A method for operating an image processing system between a reduced resolution mode and a normal resolution mode, comprising:

activating stages of an analog-to-digital converter (ADC) for an analog front end circuit of an image processing system that is operating in a normal resolution mode; and

de-activating at least some of the stages of the ADC when the image processing system is operating in a reduced resolution mode.

35. (New) The method according to Claim 34, wherein de-activating at least some of the stages of the ADC, further comprises:

de-activating lower stages which provide lower significant bits of a digital value.

36. (New) The method according to Claim 35, wherein de-activating lower stages further comprises:

setting the lower significant bits to low values wherein the lower stages in effect contain no information.

37. (New) The method according to Claim 34, wherein the reduced resolution mode is a preview operational mode and de-activating at least some of the stages of the ADC, further comprises:

de-activating stages of the ADC during the preview operational mode.

38. (New) The method according to Claim 34, further comprising:

outputting two bits from each of the stages;

outputting a bit significance of a least significant bit and a least significant bit plus one for a most significant bit stage;

outputting another bit significance of twice an output value of a subsequent stage for each of the other stages; and

outputting bits for the ADC by adding together the outputs of all of the stages.